

Fig. 1

Prior Art

20 →

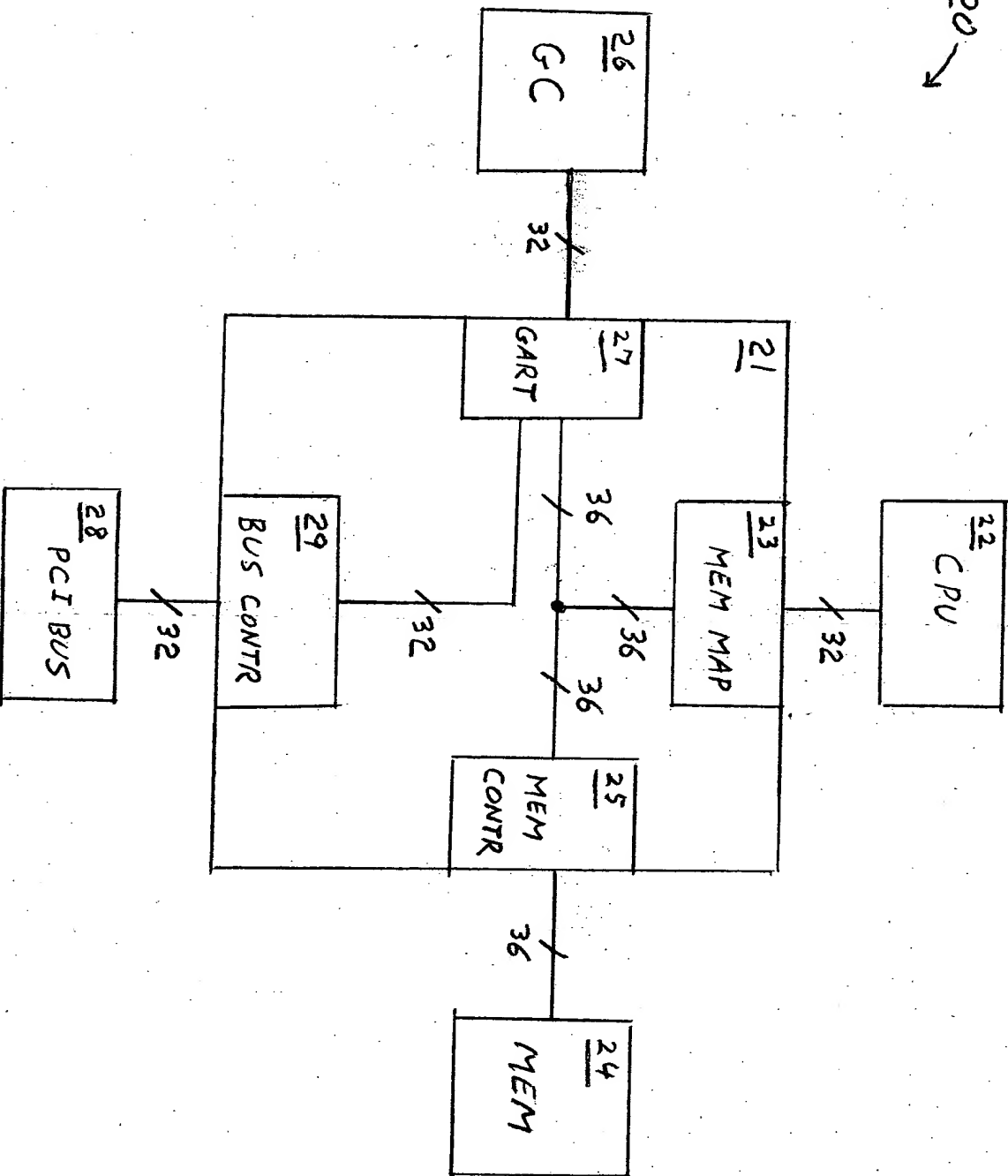


Fig. 2

FIG. 2 is a block diagram of a system architecture 20. The system architecture 20 includes a CPU 22, a system bus 21, a memory map 23, a GART 27, a GC 26, a PCI BUS 28, a MEM CONTR 25, and a MEM 24. The CPU 22 is connected to the system bus 21 via a 32-bit connection. The system bus 21 is connected to the GC 26 via a 32-bit connection. The system bus 21 is connected to the PCI BUS 28 via a 32-bit connection. The GART 27 is connected to the GC 26 via a 32-bit connection. The GART 27 is connected to the MEM CONTR 25 via a 36-bit connection. The MEM CONTR 25 is connected to the MEM 24 via a 36-bit connection.

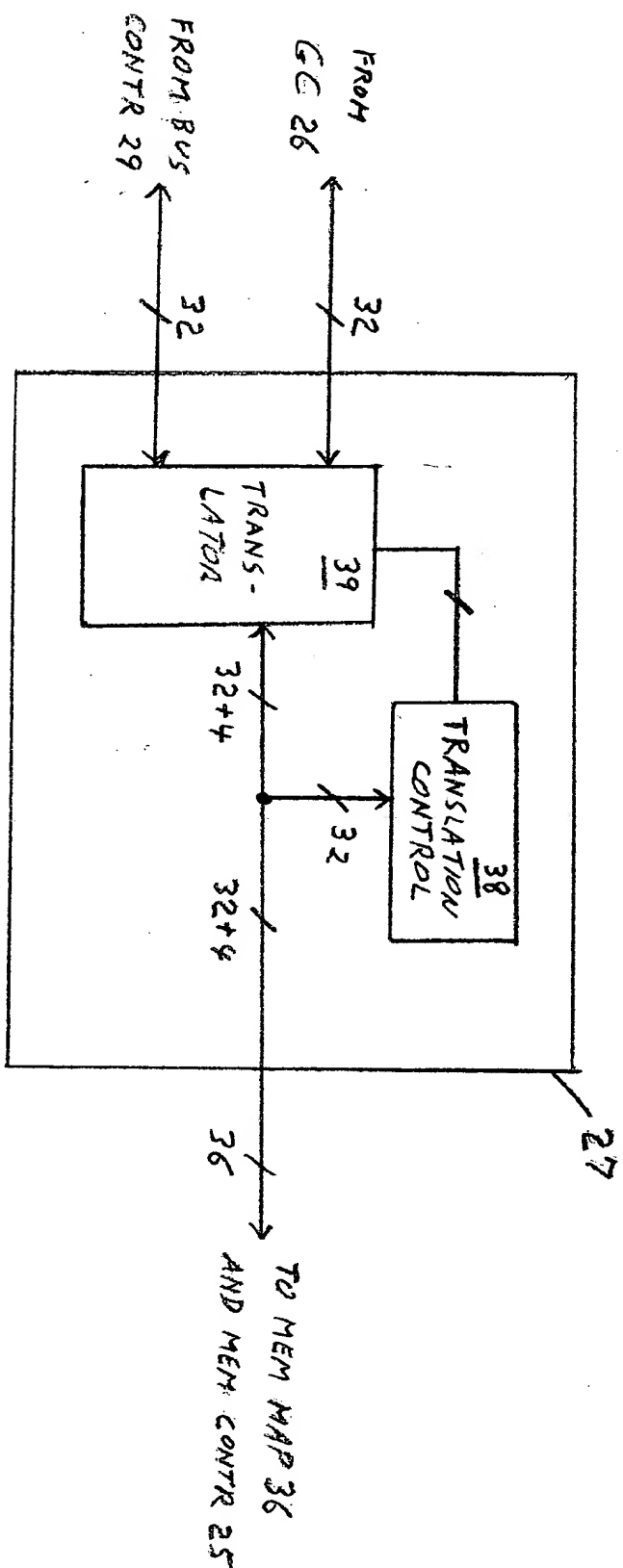


Fig. 3

Fig. 4

